



C-01-082B



February 9, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/755,495 01/12/04 |
Wei-Hua Cheng et al.
ADJUSTABLE 3D CAPACITOR
| _____ |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

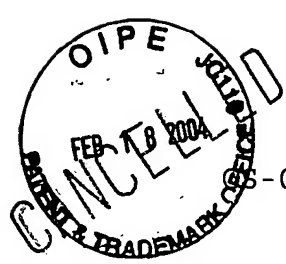
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on February 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 2/17/04



OS-01-082B



U.S. Patent 5,350,705 to Brassington et al., "Ferro-electric Memory Cell Arrangement Having a Split Capacitor Plate Structure," discloses a flat capacitor arrangement with common top plate.

U.S. Patent 6,088,258 to Aitken et al., "Structures for Reduced Topography Capacitors," discloses planarized interweave capacitor.

U.S. Patent 5,604,145 to Hashizume et al., "Method of Manufacturing DRAM Capable of Randomly Inputting/Outputting Memory Information at Random," discloses a planar capacitor process.

U.S. Patent 5,744,385 to Hojabri, "Compensation Technique for Parasitic Capacitance," reveals a compensation technique for a parasitic capacitor.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

